(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 176 711 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
30.01.2002 Bulletin 2002/05

(51) Int Cl.7: H03F 1/32

(21) Application number: 01000295.4

(22) Date of filing: 13.07.2001

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 13.07.2000 US 615377

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(54) **Apparatus and method for electrical signal amplification**

(57) An apparatus and method for utilizing a correction loop amplifier in conjunction with a main amplifier to produce signal amplification with low total harmonic distortion. The correction amplifier preferably has one input directly coupled to a first input of the main amplifier, and an output coupled to a second input of the main amplifier via a resistor. The second input of the correction amplifier is preferably coupled to a signal input via a voltage divider or RC network. A preferred embodiment configuration provides a power amplifier with improved THD over prior art circuits. The circuit is very flexible, and may incorporate low, high or band pass filter functions if desired. In addition, the power amplifier may be implemented in any combination of single or differential inputs and outputs.

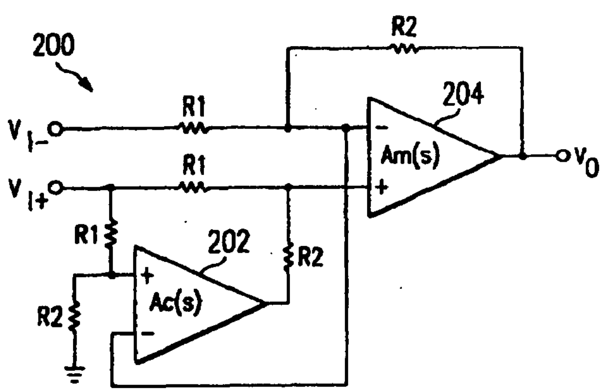

FIG. 3

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Description

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates generally to an apparatus and method for electrical signal amplification, and more particularly to an apparatus and method for utilizing a correction loop amplifier in conjunction with a main signal amplifier to reduce output signal distortion.

DESCRIPTION OF THE RELATED ART

[0002] Signal amplifiers are used in many types of electronic circuits in a wide variety of consumer, industrial and other products. One such application is a power amplifier that may be used to provide a large amount of signal amplification for audio equipment. A conventional prior art differential input power amplifier circuit is illustrated in Figure 1. One problem with this circuit, however, is that it typically has relatively high total harmonic distortion ("THD"), and thus its direct use in high performance circuits is limited.

[0003] One approach to reducing the THD in a power amplifier circuit is taught by above-referenced U.S. Patent Application No. 09/491,543 FILED 26 January 2000. Figure 2 illustrates a low THD amplifier circuit 100 as disclosed by the above-referenced patent application. The transfer function of this circuit is generally given by

$$v_O = \frac{A_m(s)[A_c(s)(1-k)+k]v_{I+} - A_m(s)kv_{I-}}{A_m(s)A_c(s)(1-k)k_2 + A_m(1-k)+1}$$
$$= \frac{\left[1+\frac{k}{A_m(s)}\right]v_{I+} - \frac{k}{A_c(s)(1-k)}v_{I-}}{k_2 + \frac{1}{A_c(s)} + \frac{1}{A_m(s)A_c(s)(1-k)}} \qquad (1)$$

where

$$k=\frac{R_2}{R_1+R_2},\ k_2=\frac{R_4}{R_3+R_4},$$

$A_m(s)$ and $A_c(s)$ are transfer functions of main amplifier 102 and correction loop amplifier 104, respectively.

[0004] Generally, to properly operate circuit 100, the output of correction amplifier 104 ($A_c(s)$) should be virtual ground. If the input is a completely fully differential signal (i.e., $v_{I+}=v_{I-}$) the following equations may be derived:

$$v_O\frac{R_4}{R_3+R_4}=v_{I+},\ \text{and}\ v_0=\frac{R_2}{R_1}(v_{I+}-v_{I-})=\frac{2R_2}{R_1}v_{I+}.$$

Thus :

$$\frac{2R_2}{R_1}=\frac{R_3+R_4}{R_4} \qquad (2)$$

[0005] Furthermore, if $R_4 = R_1$, then $R_3 = 2R_2 - R_1$.

[0006] In practical circuit design, it is generally difficult to match $R_3=2R_2-R_1$ to other resistors with values of R_1 or R_2.

[0007] If $A_m(s)$>>0, $A_c(s)$>>0 and $A_c(s)(1-k)$>>0, the above equation may be simplified to

$$v_O = \frac{v_{I+}}{k_2} = \frac{R_3 + R_4}{R_4} v_{I+} = \left(\frac{R_3}{R_4} + 1 \right) v_{I+} \quad (3)$$

[0008] This indicates that the output voltage v_o is mainly determined by the positive input v_{I+}, and is insensitive to the negative input v_{I-}. Essentially, the circuit may be operating as a single ended system, in which the input is v_{I+} and the output is v_o. Therefore, a potential disadvantage with this circuit is that it may not be operating as a fully differential structure. Generally, in a mixed-signal environment, many of the digital noises are present in the power supply, substrate, or the signal wires, in a common mode fashion. In such an environment, a fully differential structure generally provides high (digital) noise immunization, a high Common-Mode Rejection Ratio ("CMRR"), and a high Power Supply Rejection Ratio ("PSRR"). However, because of the potential singled-ended operating characteristic of the circuit of Figure 2, the benefits of a fully differential circuit may not be achieved.

[0009] For the circuit configuration shown in Figure 2, the CMRR is:

$$CMRR = \frac{A_{DM}}{A_{CM}} = \frac{{}^{vo}/(v_{I+} - v_{I-})}{{}^{vo}/(v_{I+} + v_{I-})/2} = \frac{1}{2} = -6\,dB \quad (4)$$

[0010] Another potential disadvantage with the circuit illustrated in Figure 2 is that it is relatively difficult to add a filtering function to the circuit.

SUMMARY OF THE INVENTION

[0011] These problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention comprising an apparatus and method for utilizing a correction loop amplifier in conjunction with a main amplifier to produce signal amplification with very low THD. The correction amplifier preferably has one input directly coupled to a first input of the main amplifier, and an output coupled to a second input of the main amplifier via a resistor. The second input of the correction amplifier is preferably coupled to a signal input via a voltage divider or RC network. Alternatively, the second input of the correction amplifier may be coupled to ground, typically for a single ended input negative gain configuration. A preferred embodiment configuration provides a power amplifier with improved THD over prior art circuits. The circuit is very flexible, and may incorporate low, high or band pass filter functions if desired. In addition, the power amplifier may be implemented in any combination of single or differential inputs and outputs.

[0012] In accordance with a preferred embodiment of the present invention, a power amplifier circuit apparatus comprises a main amplifier having first and second input nodes and an output node; a feedback resistor coupled between the first input node and the output node of the main amplifier; a correction loop amplifier having first and second input nodes and an output node, wherein the first input node of the correction amplifier is coupled to the first input node of the main amplifier; and a resistor coupled between the output node of the correction amplifier and the second input node of the main amplifier.

[0013] In accordance with another preferred embodiment of the present invention, a differential output amplifier circuit generates a balanced output signal having positive and negative signal components. The circuit comprises a first power amplifier circuit for providing the positive signal component of the balanced output signal, and a second power amplifier circuit for providing the negative signal component of the balanced output signal. Each of the first and second power amplifier circuits are configured similarly to the previously described embodiment.

[0014] In accordance with another preferred embodiment of the present invention, an amplifier circuit comprises a main amplifier and a correction amplifier, the main amplifier having first and second input nodes and an output node, and the correction amplifier having first and second input nodes and an output node. A method of correcting distortion in the amplifier circuit comprises feeding back an output signal from the main amplifier output node to the main amplifier first input node via a first resistor; feeding back the output signal to the correction amplifier first input node via the resistor; generating a correction signal at the output node of the correction amplifier; and providing the correction signal to the main amplifier second input node via a second resistor.

[0015] An advantage of a preferred embodiment of the present invention is that it provides much improved CMRR performance over prior art approaches. Assuming, ideal matching of resistors, and ideal main and correction amplifiers, the CMRR of the circuit should approach infinity. Practically, the CMRR of the circuit is limited by the matching of the resistors and the CMRR of the amplifiers. The higher CMRR generally provides higher immunization to digital interfer-

ence and other common mode noise.

[0016] A further advantage of a preferred embodiment of the present invention is that it provides more gain flexibility than prior art approaches. The gain may be any value that is determined by

$$\frac{R_2}{R_1},$$

so this preferred embodiment may be used to implement, for example, the volume control in the feedback loop of amplifier. For the prior art scheme discussed hereinabove, with

$$\frac{v_o}{v_{I+}}=\frac{R_3}{R_4}+1,$$

the minimum gain value is 1. Because the gain cannot be less than 1, it generally cannot be used in a volume control application.

[0017] A further advantage of a preferred embodiment of the present invention is that it provides configuration flexibility. For example, the amplifier could be configured to perform:

(1) fully-differential (balanced) input, single-ended output, 2-channel (4-channel) stereo;
(2) single-ended input, single-ended output, 2-channel (4-channel) stereo;
(3) fully-differential (balanced) input and output, mono (2-channel stereo);
(4) single-ended input, fully-differential (balanced) output, mono (2-channel stereo).

[0018] Configuration selection may be performed during design, or by using a few switches, after the circuit has been built. A basic design may be prepared beforehand, and then implemented in different configurations with a few wire connection changes.

[0019] A further advantage of a preferred embodiment of the present invention is that it is relatively easy to match all of the resistors, because each of the resistors is assigned one of two values.

[0020] A further advantage of a preferred embodiment of the present invention is that it is easy to extend the circuit to perform low pass, high pass, or band pass filter functions.

[0021] A further advantage of a preferred embodiment of the present invention is that it has extremely low THD compared with a conventional amplifier configuration.

[0022] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWING

[0023] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following detailed description of certain particular and illustrative embodiments and the features and aspects thereof, by way of example only, and with reference to the figures of the accompanying drawings in which:

FIGURE 1 is a schematic diagram of a prior art amplifier;
FIGURE 2 is a schematic diagram of an amplification circuit comprising a correction amplifier with an input coupled to an output of a main amplifier via a voltage divider;
FIGURE 3 is a schematic diagram of a preferred embodiment circuit comprising a correction amplifier with a input directly coupled to an input of a main amplifier;
FIGURE 4 is a signal flow diagram of the circuit in Figure 3;
FIGURE 5 is a schematic diagram of a preferred embodiment low pass filter;
FIGURE 6 is a schematic diagram of a preferred embodiment high pass filter;
FIGURE 7 is a schematic diagram of a preferred embodiment band pass filter;
FIGURE 8 is a schematic diagram of a positive gain single ended input configuration;

FIGURE 9 is a schematic diagram of a negative gain single ended input configuration;
FIGURE 10 is a schematic diagram of a single ended input, balanced output configuration;
FIGURE 11 is a schematic diagram of a balanced input and output configuration;
FIGURE 12 is a schematic diagram of a main amplifier;
FIGURE 13 is a schematic diagram of a correction amplifier;
FIGURE 14 is a schematic diagram of a preferred embodiment power amplifier; and
FIGURE 15 is a graph of signal/distortion ratio versus frequency.

DETAILED DESCRIPTION

[0024] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0025] The present invention will be described with respect to preferred embodiments in a specific context, namely a power amplifier configuration for use as an audio amplifier. The invention may also be applied, however, to other systems requiring electrical signal amplification. The circuit may be implemented with extremely low THD and used in high-end high-fidelity audio power amplifier chips. As another example, it may be used in low power codecs. For low-end applications that do not require high THD performance, higher THD may be traded off for lower power consumption. This relatively higher THD may still be at a level of performance comparable with that of conventional power amplifier designs. As another example, the low THD amplifier topology is generally process independent, so it may be used in any audio amplifier design implemented in CMOS, bipolar, or BiCMOS integrated circuits. It may also be implemented in a discrete component design, for example, for high-end audio power amplifier systems.

[0026] A schematic of a preferred embodiment double feedback loop fully differential to single ended amplifier is shown in Figure 3, and the associated signal flow diagram 250 is shown in Figure 4. The transfer function of this topology may be derived as follows. Assume both $A_c(s)$ correction loop amplifier 202 and $A_m(s)$ main amplifier 204 are 2-pole amplifiers, and their transfer functions are

$$A_m(s)=\frac{A_{m0}}{\frac{s^2}{f_{m2}p_{m1}}+\frac{s}{p_{m1}}+1}, \tag{5a}$$

and

$$A_c(s)=\frac{A_{c0}}{\frac{s^2}{f_{c2}p_{c1}}+\frac{s}{p_{c1}}+1}. \tag{5b}$$

[0027] Defining $k=\frac{R_2}{R_1+R_2}$, the output voltage may be obtained as

$$v_0(s)=\frac{kA_m(s)[1+A_c(s)(1-k)]}{1+A_m(s)A_c(s)(1-k)^2+A_m(s)(1-k)}(v_{i+}-v_{i-}) \tag{6a}$$

[0028] In other words, the transfer function is

$$H(s)=\frac{v_o(s)}{v_{i+}-v_{i-}}=\frac{kA_m(s)[1+A_c(s)(1-k)]}{1+A_m(s)A_c(s)(1-k)^2+A_m(s)(1-k)} \tag{6b}$$

[0029] The most stringent condition for stability occurs when k = 0, at which point the amplifier effectively works in a unity gain feedback configuration as a non-inverting amplifier. The gain of the amplifier then reduces to

$$H(s)=\frac{kA_m(s)[1+A_c(s)]}{1+A_m(s)A_c(s)+A_m(s)} \tag{7}$$

[0030] $A_m(s)$ and $A_c(s)$ are then substituted with Equations (5a) and (5b). By multiplying the denominators of $A_m(s)$ and $A_c(s)$ for both of the numerator and denominator of Equation (7), the denominator of $H(s)$ may be obtained as

$$D_H(s)=\left(\frac{s^2}{f_{m2}p_{m1}}+\frac{s}{p_{m1}}+1\right)\left(\frac{s^2}{f_{c2}p_{c1}}+\frac{s}{p_{c1}}+1\right)+A_{m0}A_{c0}+A_{m0}\left(\frac{s^2}{f_{c2}p_{c1}}+\frac{s}{p_{c1}}+1\right)$$

$$=A_{m0}A_{c0}\left[\begin{array}{l}\dfrac{s^4}{f_{m2}f_{m1}f_{c2}f_{c1}}+s^3\dfrac{1}{f_{m1}f_{c1}}\left(\dfrac{1}{f_{m2}}+\dfrac{1}{f_{c2}}\right)+s^2\left(\dfrac{1}{f_{m2}f_{m1}A_{c0}}+\dfrac{1}{f_{c2}f_{c1}A_{m0}}+\dfrac{1}{f_{m1}f_{c1}}+\dfrac{1}{f_{c2}f_{c1}}\right)\\+s\left(\dfrac{1}{f_{m1}A_{c0}}+\dfrac{1}{f_{c1}A_{m0}}+\dfrac{1}{f_{c1}}\right)+\left(1+\dfrac{1}{A_{m0}A_{c0}}+\dfrac{1}{A_{c0}}\right)\end{array}\right]$$

$$\underline{\underline{A_{m0}\gg 1,\,A_{c0}\gg 1}}\quad A_{m0}A_{c0}\left[\frac{s^4}{f_{m2}f_{m1}f_{c2}f_{c1}}+s^3\frac{1}{f_{m1}f_{c1}}\left(\frac{1}{f_{m2}}+\frac{1}{f_{c2}}\right)+s^2\frac{1}{f_{c1}}\left(\frac{1}{f_{m1}}+\frac{1}{f_{c2}}\right)+s\frac{1}{f_{c1}}+1\right] \tag{8}$$

[0031] In a preferred embodiment, the transfer characteristic of Fig. 3 is given by

$$v_0(s)=\frac{kA_m(s)[1+A_c(s)(1-k)]}{1+A_m(s)A_c(s)(1-k)^2+A_m(s)(1-k)}(v_{i+}-v_{i-})=\frac{k}{1-k}(v_{i+}-v_{i-})=\frac{R_2}{R_1}(v_{i+}-v_{i-}) \tag{9}$$

[0032] Ideally, if the main and correction amplifiers have very high CMRR and the R1s and R2s are closely matched, then this topology should not introduce any CMRR degradation into the system, and higher immunization to digital interference and other common mode noise should be expected.

[0033] To examine stability conditions, it is useful to compare Equation (8) above with Equation (9) in the document, F. You et al., "Multistage amplifier topologies with nested Gm-C compensation," IEEE J. Of Solid-State Circuits, vol. 32, no.21, pp. 2000-2011 (Dec. 1997), which document is hereby incorporated herein by reference. Using these equations, the following may be obtained:

$$f_1=f_{c1}, \tag{10a}$$

$$f_2=\frac{f_{m1}f_{c2}}{f_{m1}+f_{c2}}, \tag{10b}$$

$$f_3=\frac{(f_{m1}+f_{c2})f_{m2}}{f_{m2}+f_{c2}} \tag{10c}$$

$$f_4=f_{m2}+f_{c2} \tag{10d}$$

where $f_{m1}=p_{m1}A_{m0}$ and $f_{c1}=p_{c1}A_{c0}$ are the unity gain frequencies of the main and correction amplifiers, and the f_i (i = 1 to 4) are the equivalent frequencies of the nested transconductance-capacitance compensation ("NGCC") amplifier of F. You et al.

[0034] Although the Routh stability criterion may be applied directly to obtain the stability requirements, it is generally very complex and requires significant mathematical work. According to F. You et al., the stability condition is given by

$$f_4>f_2,\text{ and } f_4>f_2\frac{1}{1-f_1/f_3}.$$

[0035] That is, for the preferred embodiment amplifier in Figure 3, the stability condition is:

$$f_{m2}+f_{c2}>\frac{f_{m1}f_{c2}}{f_{m1}+f_{c2}}, \tag{11a}$$

and

$$f_{m2}+f_{c2}>\frac{f_{m1}f_{m2}f_{c2}}{f_{m2}(f_{c2}+f_{m1})-f_{c1}(f_{c2}+f_{m2})} \tag{11b}$$

[0036] Because equation (11a) is generally always true, equation (11b) becomes the only requirement for stability.

[0037] If f_{c1} = 1*MHz*, f_{c2} =3*MHz*, f_{m1} =3*MHz*, and f_{m2} = 6*MHz*, the following values may be obtained: f_1=1*MHz*, f_2=1.5*MHz*, f_3=4*MHz*, and f_4 =9*MHz*.

[0038] Examining the THD of the circuit shown in Figure 3, the THD is primarily dependent on the total gain of the feedback loop. As a rule of thumb, the THD improvement is given by

$$THD=-20\log\left[\left(\frac{f_{c1}f_{m1}}{f_H^2}\right)(1-k)^2\right], \tag{12}$$

where f_H is the highest working frequency of the amplifier. For example for audio compact disc player amplifiers, f_H should be about 20KHz.

[0039] In accordance with other preferred embodiments, filtering functions, such as low pass, high pass, and band pass may be incorporated into the amplifier. The low pass filter function may be particularly useful for some applications because it is desirable to eliminate some high frequency component switched-capacitor noise or D/A converter noise at sample frequency.

(1) Low pass filter. For a 1st order low pass filter, a capacitor (C2) 302 is added in parallel with every R2 304 in amplifier circuit 300 illustrated in Figure 5. The low pass transfer function is roughly given by:

$$A_{LP}(s)=\frac{R_2}{R_1}\frac{1}{1+s/p_2} \tag{13}$$

where p_2 is the -3dB angular frequency, which is given by $p_2=\frac{1}{R_2C_2}$. The -3dB frequency (in Hz) is, $f_{-3dB}=\frac{p_2}{2\pi}=\frac{1}{2\pi R_2C_2}$.

(2) High pass filter. For a 1st order high pass filter, a capacitor (C1) 332 is added in series with every R1 334 in amplifier circuit 330 illustrated in Figure 6. The high pass transfer function is generally given by:

$$A_{HP}(s)=\frac{R_2}{R_1}\frac{s}{1+s/p_1} \tag{14}$$

where p_1 is the -3dB high pass angular frequency, which is given by $p_1=\frac{1}{R_1C_1}$.

(3) Band pass filter. For a 1st order band pass filter, the low pass and high pass implementations may be combined together. In other words, a capacitor (C2) 362 is added in parallel with every R2 364, and a capacitor (C1) 366 is added in series with every R1 368, in amplifier circuit 360 illustrated in Figure 7. The band pass transfer function is generally given by:

$$A_{BP}(s)=\frac{R_2}{R_1}\frac{s}{(1+s/p_1)(1+s/p_2)} \tag{15}$$

where

$$p_1 = \frac{1}{R_1C_1}$$

and

$$p_2 = \frac{1}{R_2C_2}.$$

[0040] Alternatively, if the square wave transient response is desirable for a particular application, a small capacitor C2 (e.g., C2 = 10p, and R2 = 50K) may be beneficial.

[0041] In accordance with other preferred embodiments, the circuit topology described above may be implemented in configurations other than fully-differential to single-ended. For example, by shorting one input to analog ground, a single-ended to single-ended configuration may be configured. Depending on which input is shorted to ground, the gain may be positive or negative, as illustrated in Figures 8 & 9. Figure 8 illustrates single-ended to single-ended power amplifier 400 with positive gain, while Figure 9 illustrates single-ended to single-ended power amplifier 420 with negative gain.

[0042] In accordance with other preferred embodiments, the amplifier may be configured as singled-ended input, fully-differential (balanced) output amplifier 440, as shown in Figure 10, or as fully-differential (balanced) input-output amplifier 460, as illustrated in Figure 11. The circuit in Figure 10 effectively combines the positive gain amplifier of Figure 8 with the negative gain amplifier of Figure 9 to provide a fully differential output. Similarly, the circuit of Figure 11 effectively combines two amplifiers of the embodiment illustrated in Figure 3, with the inputs reversed into one of the amplifiers.

[0043] As one of ordinary skill in the art would readily appreciate, there are many possible transistor level implementations for the main and correction amplifiers. Figure 12 illustrates a preferred transistor level implementation 500 for main amplifier 204, and Figure 13 illustrates a preferred transistor level implementation 502 for correction amplifier 202. Figure 14 illustrates schematic 504 of a preferred embodiment amplifier in a fully-differential to single-ended scheme configuration.

[0044] Referring now to Figure 15, graph 600 illustrates simulation results of signal to distortion ratio versus frequency. In the simulation, $R_L = 32\Omega$, $V_{sup} = 2.5V$, and $V_{out} = 2.0\ V_{p\text{-}p}$. Curve 602 represents the signal to distortion ratio for preferred embodiment amplifier circuit 504 in Figure14, while curve 604 represents the signal to distortion ratio of the prior art circuit of Figure 1. Advantageously, curve 602 shows a 28dB - 50dB improvement over curve 604.

[0045] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, many of the features and functions discussed above can be implemented in software, hardware or firmware, or a combination thereof, running on one or more computers. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention.

Claims

1. A power amplifier circuit comprising:

a main amplifier having first and second input nodes and an output node;
a feedback resistor coupled between said first input node and said output node of said main amplifier;
a correction loop amplifier having first and second input nodes and an output node, wherein said first input node of said correction amplifier is coupled to said first input node of said main amplifier; and
a first resistor coupled between said output node of said correction amplifier and said second input node of said main amplifier.

2. The circuit of claim 1, further comprising:

   a second resistor coupled between said second input node of said correction amplifier and said second input node of said main amplifier.

3. The circuit of claim 1 or claim 2, wherein said power amplifier circuit comprises:

   a differential signal input having a first signal input node and a second signal input node.

4. The circuit of claim 3, further comprising:

   a third resistor coupled between said second input node of said correction amplifier and said first signal input node.

5. The circuit of claim 4, further comprising:

   a fourth resistor coupled between said second input node of said main amplifier and said first signal input node.

6. The circuit of claim 5, further comprising a fifth resistor coupled between said first input node of said main amplifier and said second signal input node.

7. The circuit of any of claims 3 to 6, wherein said power amplifier circuit is configured as a filter type selected from the group consisting of: low pass, high pass, and band pass.

8. The circuit of any preceding claim, wherein said power amplifier circuit comprises a single ended signal input.

9. The circuit of claim 8, further comprising:

   a fourth resistor coupled between said second input node of said main amplifier and said single ended signal input, wherein said power amplifier circuit provides positive gain.

10. The circuit of claim 9, further comprising:

    a fifth resistor coupled between said first input node of said main amplifier and said single ended signal input, wherein said power amplifier circuit provides negative gain.

11. The circuit of any preceding claim, wherein said power amplifier circuit has a gain of less than one.

12. The circuit of any preceding claim, wherein said power amplifier circuit is implemented as an integrated circuit.

13. A differential output amplifier circuit for generating a balanced output signal having positive and negative signal components, which circuit comprising:

    a first power amplifier circuit for providing said positive signal component of said balanced output signal, said first power amplifier circuit comprising
    a first main amplifier having first and second input nodes and an output node;
    a first feedback resistor coupled between said first input node and said output node of said first main amplifier;
    a first correction loop amplifier having first and second input nodes and an output node, wherein said first input node of said first correction amplifier is coupled to said first input node of said first main amplifier; and
    a first resistor coupled between said output node of said first correction amplifier and said second input node of said first main amplifier; and
    a second power amplifier circuit for providing said negative signal component of said balanced output signal, said second power amplifier circuit comprising
    a second main amplifier having first and second input nodes and an output node;
    a second feedback resistor coupled between said first input node and said output node of said second main amplifier;
    a second correction loop amplifier having first and second input nodes and an output node, wherein said first input node of said second correction amplifier is coupled to said first input node of said second main amplifier;

and
a second resistor coupled between said output node of said second correction amplifier and said second input node of said second main amplifier.

14. The circuit of claim 13, wherein said power amplifier circuit comprises:

a differential signal input having a first signal input node and a second signal input node.

15. The circuit of claim 13, wherein said power amplifier circuit comprises:

a single ended signal input.

16. A method of correcting distortion in an amplifier circuit, the amplifier circuit comprising a main amplifier and a correction amplifier, the main amplifier having first and second input nodes and an output node, the correction amplifier having first and second input nodes and an output node, said method comprising:

feeding back an output signal from said main amplifier output node to said main amplifier first input node via a first resistor;
feeding back said output signal to said correction amplifier first input node via said resistor;
generating a correction signal at said output node of said correction amplifier; and
providing said correction signal to said main amplifier second input node via a second resistor.

17. The method of claim 16, further comprising:

receiving a differential signal input at said main amplifier first and second input nodes.

18. The method of claim 17, further comprising:

said power amplifier circuit filtering said differential signal input, said filtering selected from the group consisting of: low pass, high pass, and band pass.

19. The method of any of claims 16 to 18, further comprising:

receiving a single ended signal input at one of said main amplifier first and second input nodes.

20. The method of any of claims 16 to 19, wherein said power amplifier circuit performs negative gain on an input signal.

21. The method of any of claims 16 to 20, wherein said gain is less than one.

22. The method of any of claims 16 to 21, further comprising:

generating a single ended signal output.

23. The method of any of claims, further comprising:

generating a differential signal output.

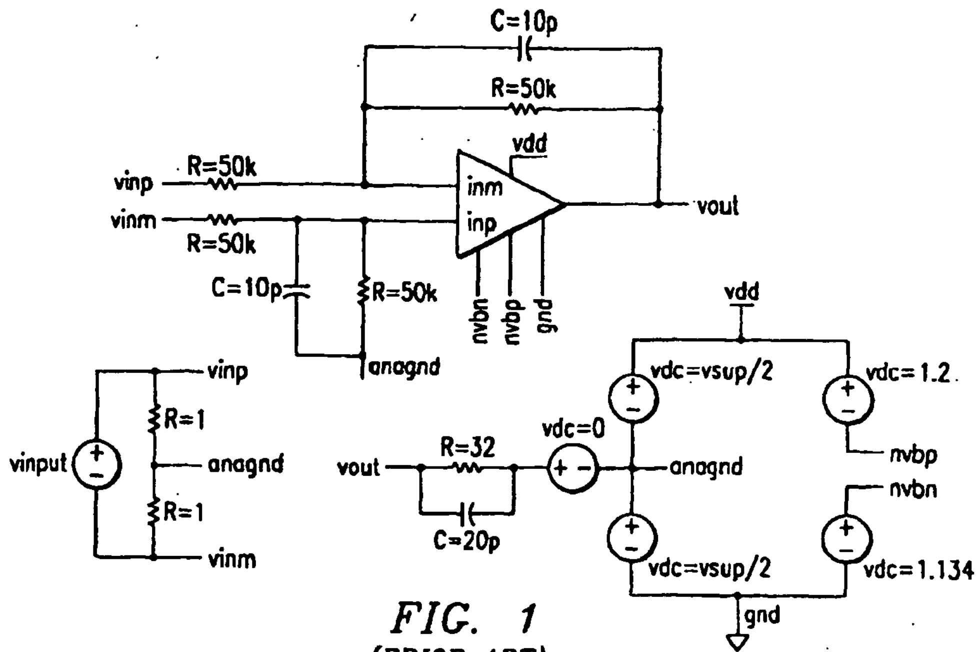


FIG. 1
(PRIOR ART)

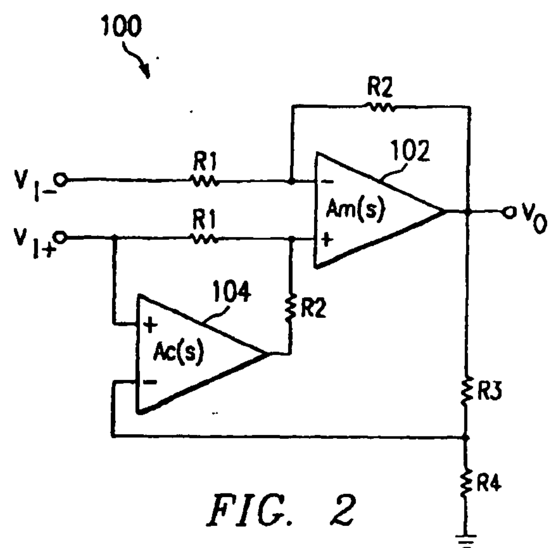


FIG. 2

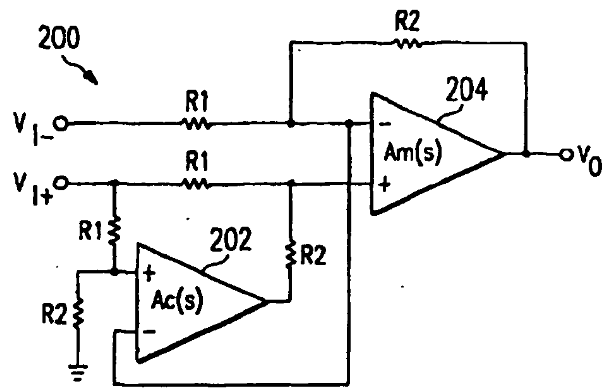


FIG. 3

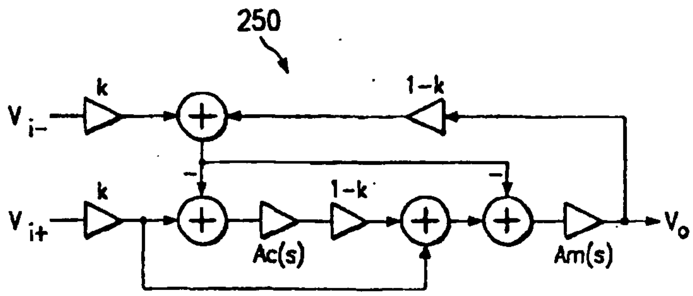


FIG. 4

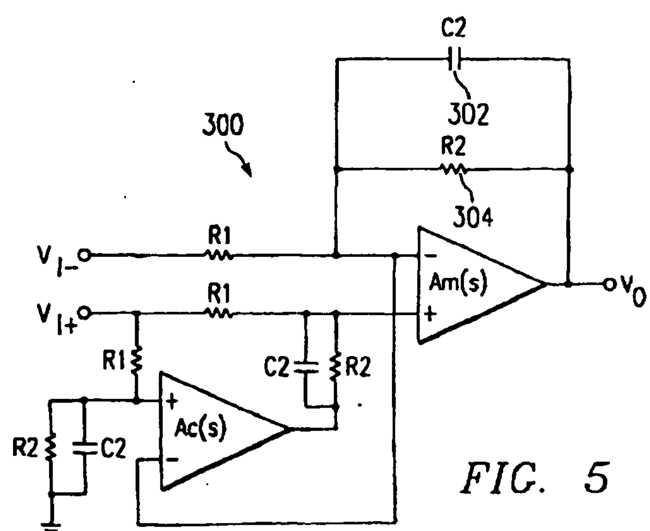


FIG. 5

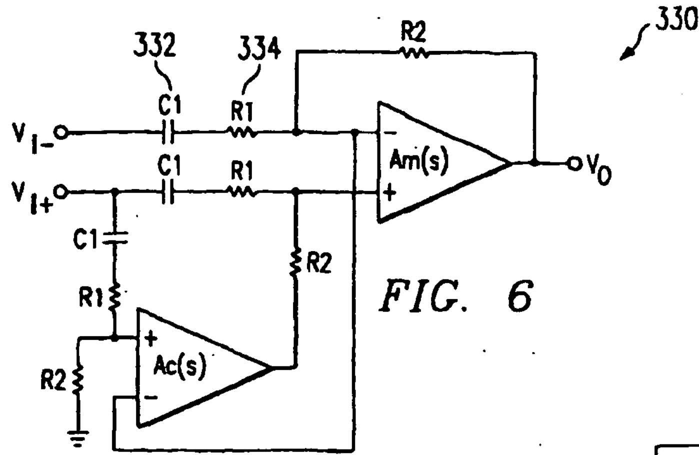


FIG. 6

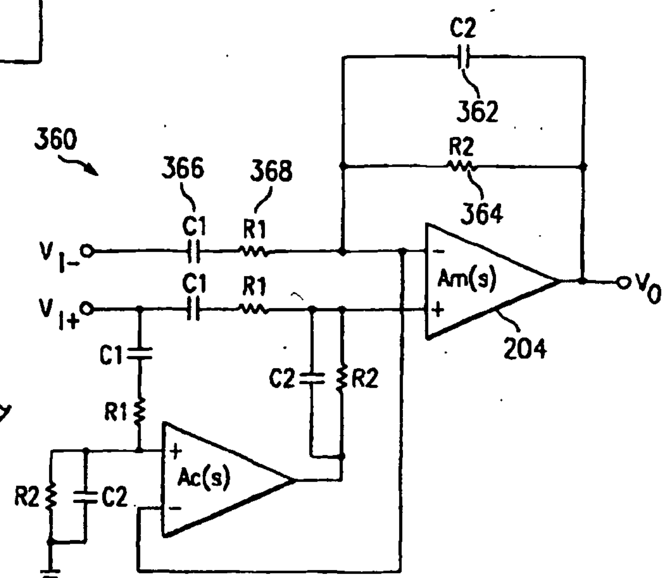


FIG. 7

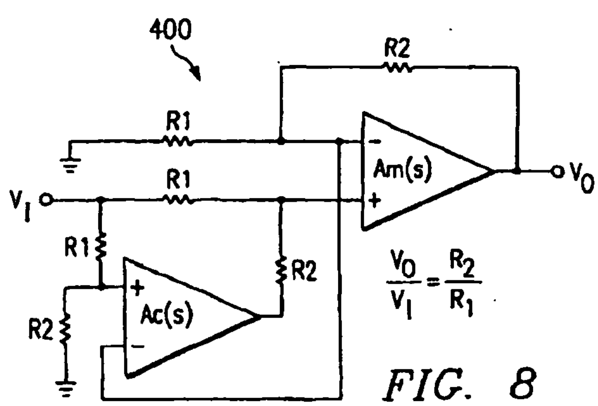


FIG. 8

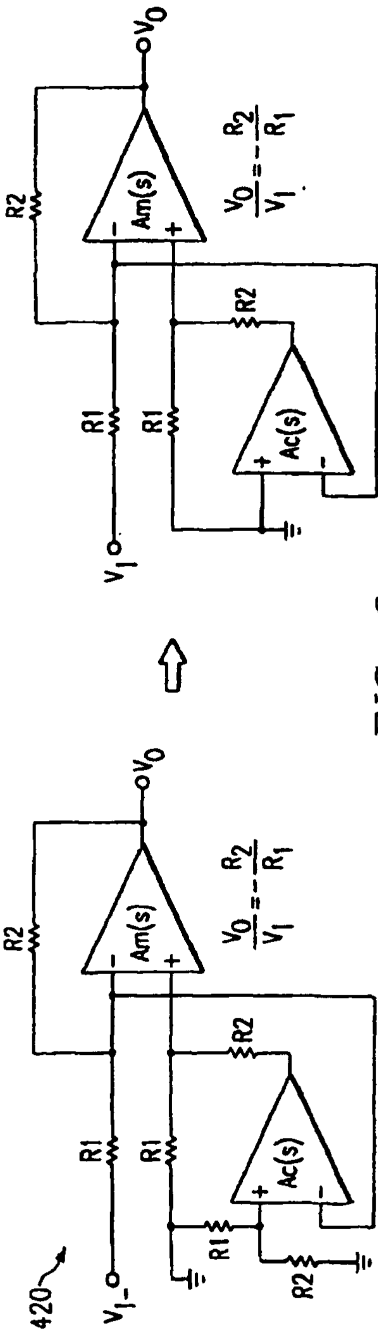

420
V_{I-}
R1
R1
R2
R1
R2
R2
Ac(s)
Am(s)
V_O
$\frac{V_O}{V_I} = -\frac{R_2}{R_1}$
V_I
R1
R1
R2
R2
Ac(s)
Am(s)
V_O
$\frac{V_O}{V_I} = -\frac{R_2}{R_1}$

FIG. 9

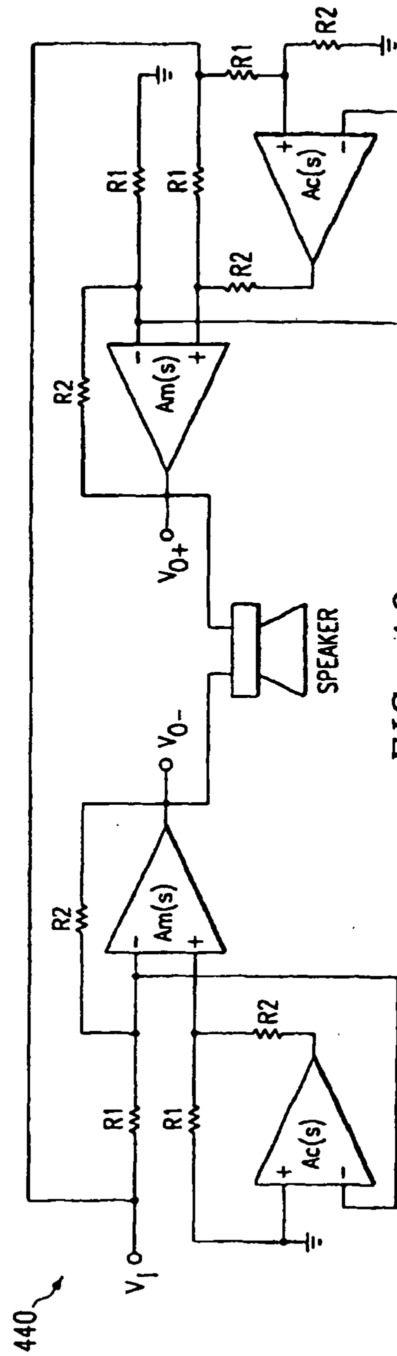

440
V_I
R1
R1
R2
R2
Ac(s)
Am(s)
V_{O-}
SPEAKER
V_{O+}
Am(s)
R2
R1
R1
R2
R1
R2
Ac(s)

FIG. 10

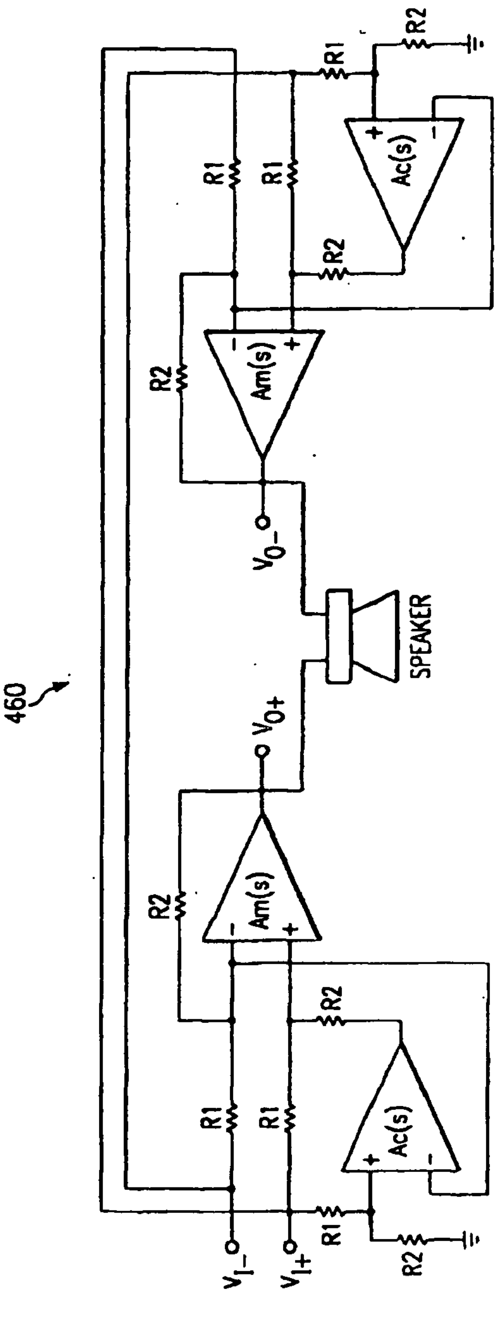


FIG. 11

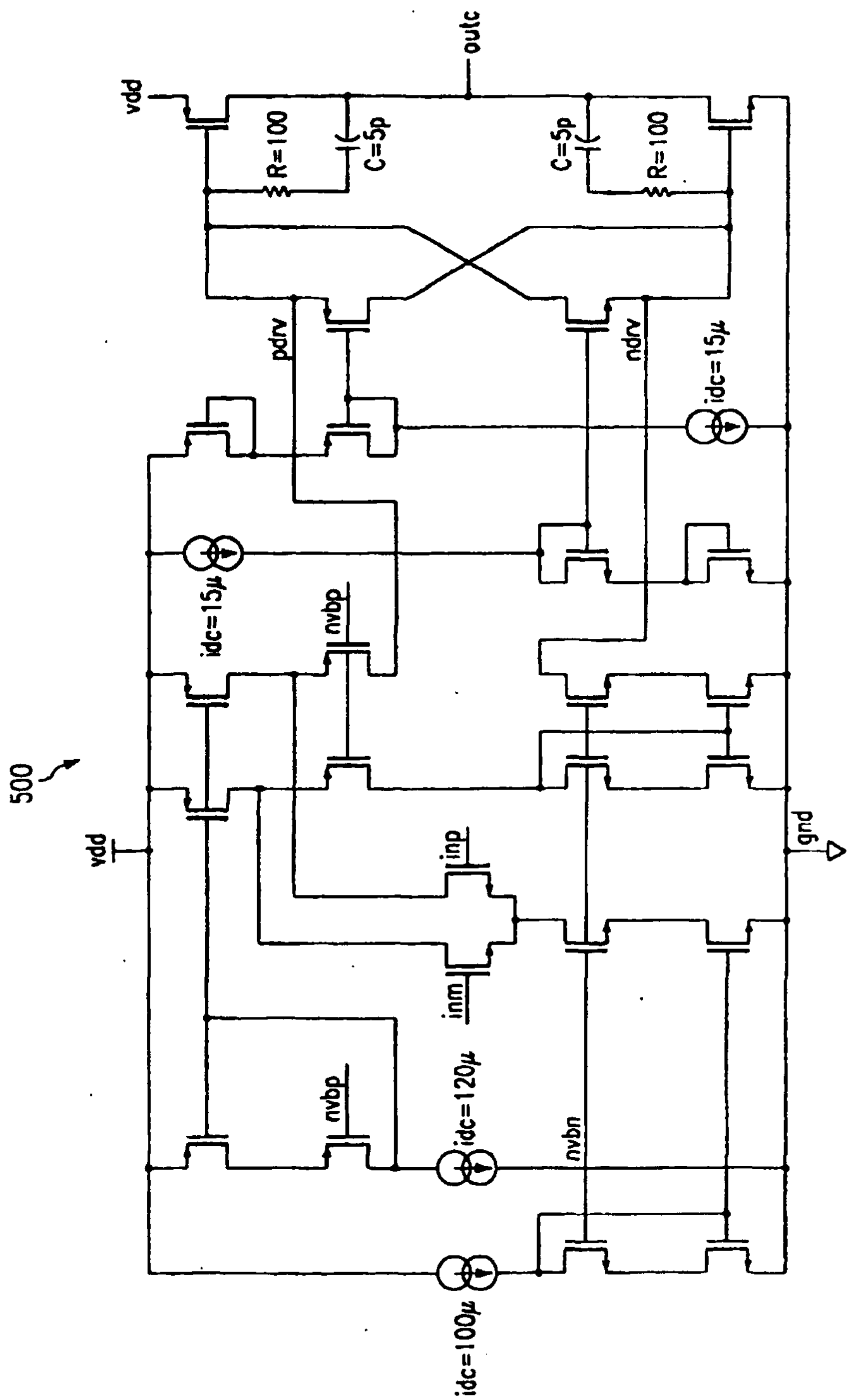

500
vdd
outc
R=100
C=5p
C=5p
R=100
pdrv
ndrv
idc=15μ
idc=15μ
nvbp
inp
inm
nvbp
idc=120μ
nvbn
idc=100μ
vdd
gnd

FIG. 12

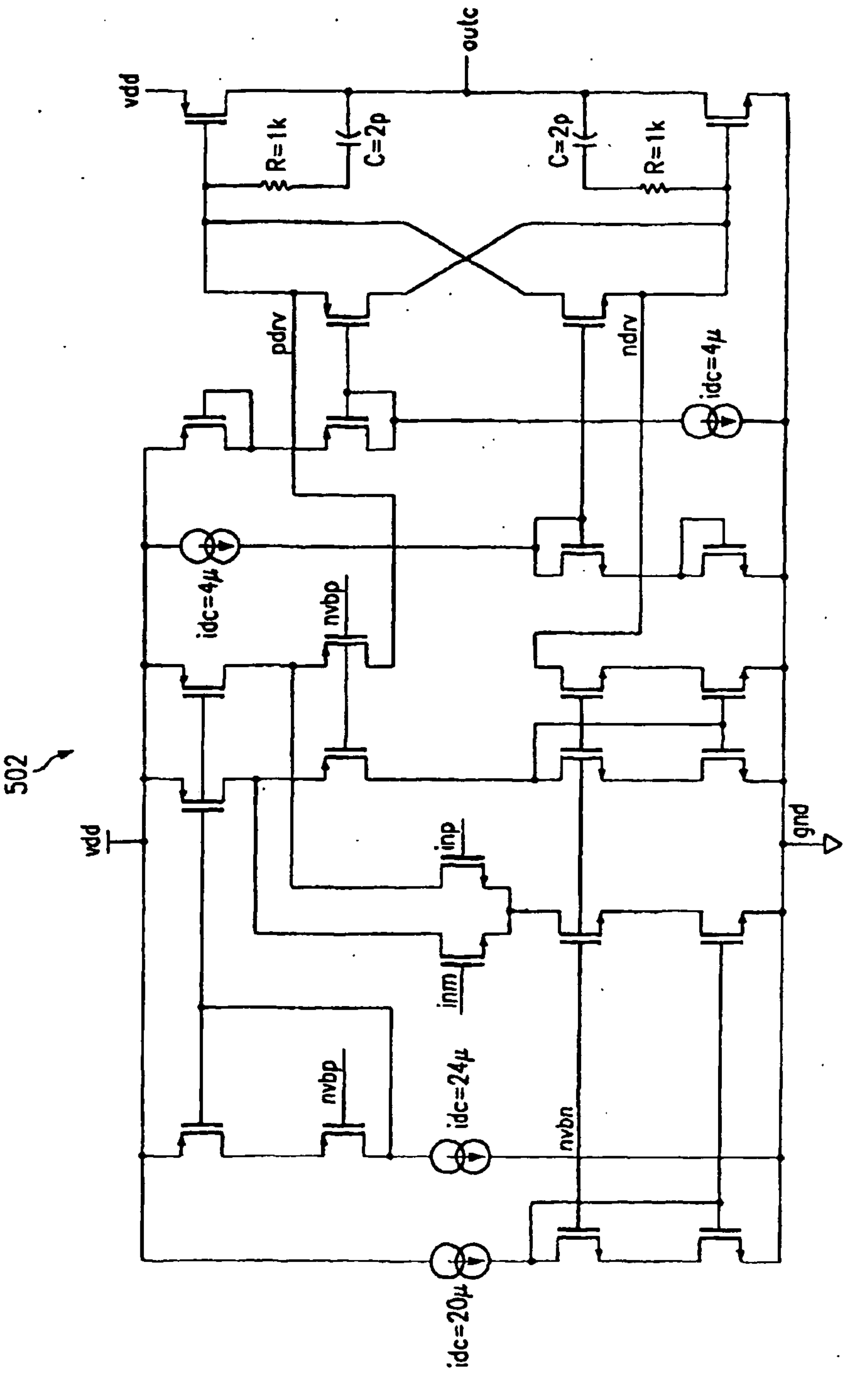

502
vdd
vdd
outc
R=1k
C=2p
C=2p
R=1k
pdrv
ndrv
idc=4μ
idc=4μ
nvbp
inp
inm
nvbp
idc=24μ
nvbn
idc=20μ
gnd

FIG. 13

FIG. 14

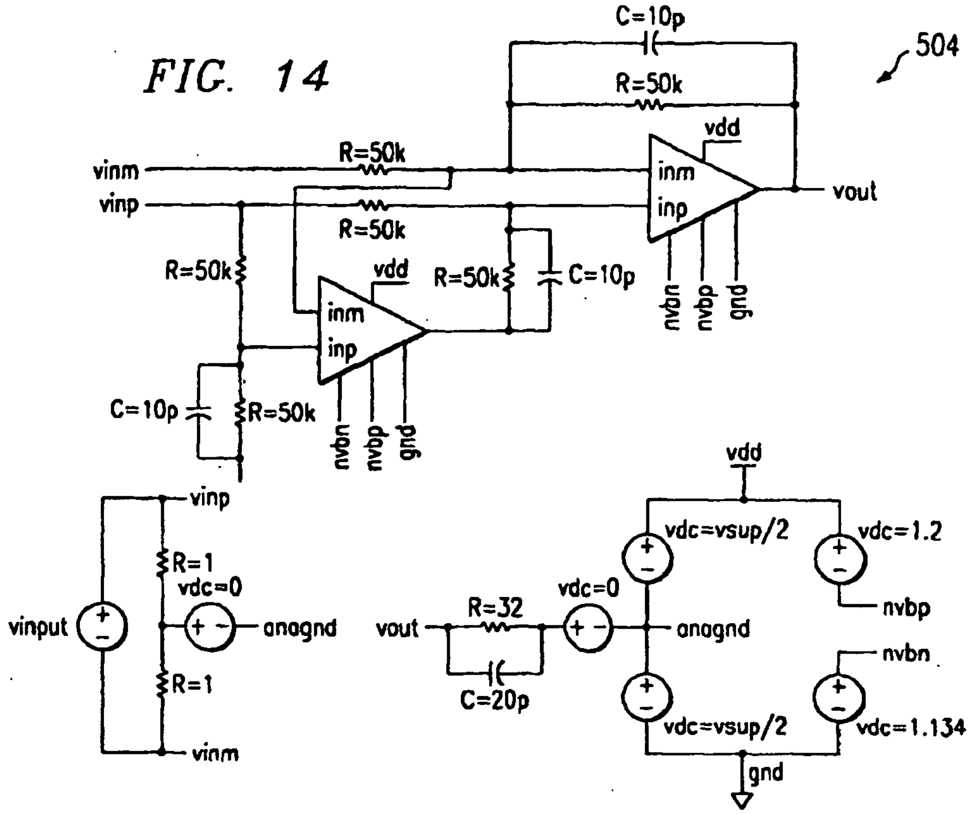
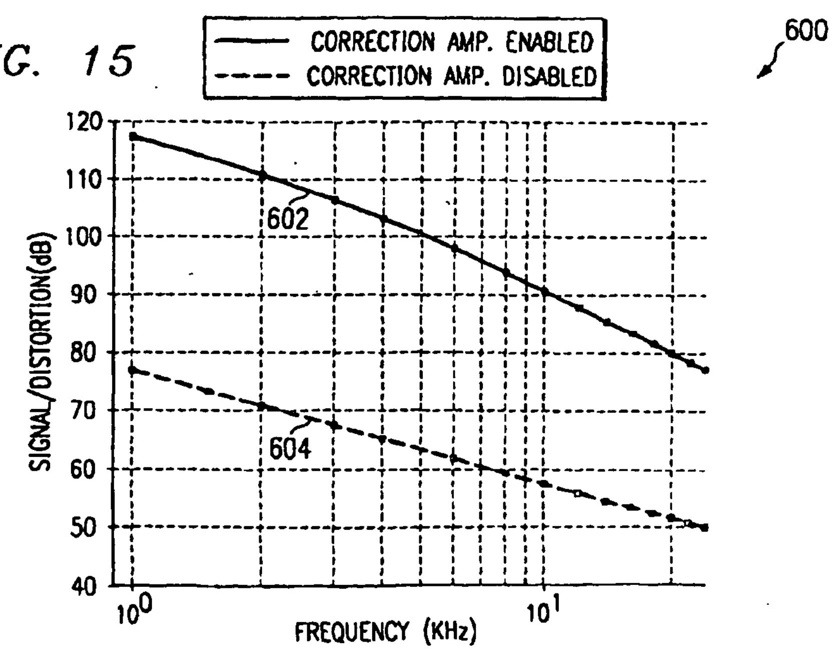

504
C=10p
R=50k
vdd
vinm
vinp
R=50k
R=50k
inm
inp
vout
R=50k
vdd
R=50k
C=10p
inm
inp
nvbn
nvbp
gnd
C=10p
R=50k
nvbn
nvbp
gnd
vinp
R=1
vdc=0
vinput
anagnd
R=1
vinm
vdd
vdc=vsup/2
vdc=1.2
vdc=0
R=32
nvbp
vout
anagnd
nvbn
C=20p
vdc=vsup/2
vdc=1.134
gnd

FIG. 15


600
CORRECTION AMP. ENABLED
CORRECTION AMP. DISABLED
SIGNAL/DISTORTION(dB)
120
110
100
90
80
70
60
50
40
602
604
10^0
10^1
FREQUENCY (KHz)